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Fabrication and electrical characterization of sub-micron diameter through-silicon via for heterogeneous three-dimensional integrated circuits

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Abstract

This paper presents the fabrication and electrical characterization of high aspect-ratio (AR) sub-micron diameter through silicon vias (TSVs) for densely interconnected three-dimensional (3D) stacked integrated circuits (ICs). The fabricated TSV technology features an AR of 16:1 with 680 nm diameter copper (Cu) core and 920 nm overall diameter. To address the challenges in scaling TSVs, scallop-free low roughness nano-Bosch silicon etching and direct Cu electroplating on a titanium-nitride (TiN) diffusion barrier layer have been developed as key enabling modules. The electrical resistance of the sub-micron TSVs is measured to be on average 1.2 Ω, and the Cu resistivity is extracted to be approximately 2.95 $\mu\Omega$ cm. Furthermore, the maximum achievable current-carrying capacity (CCC) of the scaled TSVs is characterized to be approximately 360 μA for the 680 nm Cu core.

Keywords: 3D heterogeneous integration, through-silicon-via (TSV), current carrying capacity, parasitic resistance, interconnection

(Some figures may appear in colour only in the online journal)

1. Introduction

The continuous demand for denser integration, lower power consumption, and higher bandwidth density requires developing increasingly complex interconnect technologies [1]. For instance, three-dimensional integration (3DI) is being explored as an innovative approach [2] to address the relentless need for dense interconnects with lower latency and energy dissipation through shortening the length of interconnects [3, 4]. One form of 3DI is enabled by vertically stacked silicon tiers and interconnected using through-silicon-via (TSV). This approach represents promising technology to keep pace with Moore's law [5] and incorporates the modular design benefits of a heterogeneous architecture [6]. TSV geometry, especially diameter, largely determines the electrical attributes and mechanical reliability of the interconnects as well as the 3D stack and motivates the need for scaling TSVs dimensions. For example, a 10 μm long on-chip wire with a 10 μm diameter TSV exhibits a 30 ps delay while the same length on-chip wire with a 5 μm diameter TSV exhibits an approximate latency of 10 ps [7]. Moreover, reducing the TSV diameter can significantly mitigate the stresses related to copper (Cu) expansion as the mechanical stress is proportional to the square of the TSV radius. Relieving the mechanical stress is further beneficial as it results in a smaller keep-out-zone (KoZ) [8]—which is designed to guard active devices against the adverse proximity effects of TSVs [9].

Scaling TSVs is challenging as the fabrication of smaller diameters using conventional processes faces limitations [10]. This is due to the strong dependency of both the via etch rate and metallization processes on the via aspect-ratio (AR) and diameter. A diffusion-barrier and conductive seed-layer deposition as the first steps of metallization are typically preformed using magnetron sputtering deposition [11, 12]. However, this method of material deposition is not effective for the fabrication of high AR scaled TSVs as it may cause the TSV opening diameter to decrease before the via sidewall is fully coated

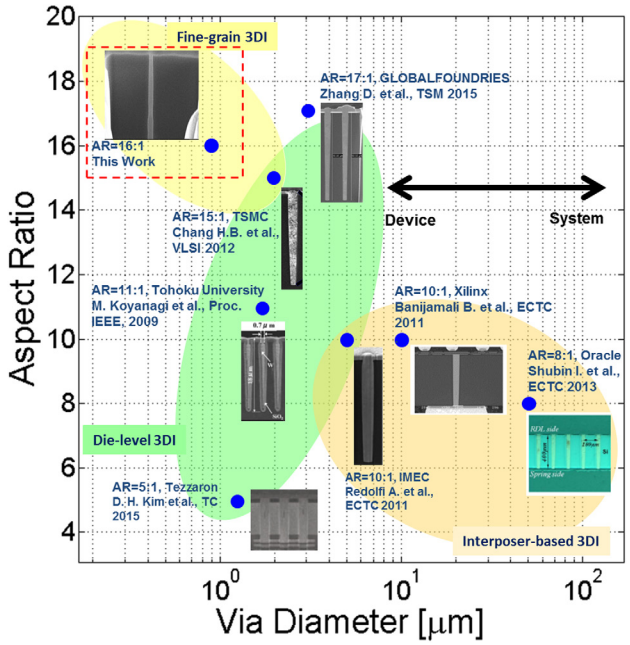

Figure 1. TSV aspect ratio versus diameter for TSVs in the literature.

[10]. This issue is caused by prolonged sputter deposition time, which is necessary to ensure continuous film formation as the material flux density at the bottom of TSV is limited.

Despite the relentless efforts to reduce TSV footprint [3, 13–18], virtually no results have been reported for high AR (greater than 10:1) Cu TSVs (based on superfilling) in bulk silicon with total diameters below one micron, as shown in figure 1. In this paper, TSVs with sub-micron diameter and 16:1 AR are fabricated and characterized. The fabrication process presented in section 2 discusses the key enabling modules developed for scaling TSV technology. This includes 1-development of low roughness and scallop-free nano-Bosch silicon etching, and 2-a demonstration of void-free Cu electrodeposition directly on a titanium nitride (TiN) diffusion barrier film. Lastly, the electrical resistance and ampacity of the fabricated sub-micron TSVs are measured using the 4-wire Kelvin probe technique.

2. Fabrication

2.1. Electron beam lithography (EBL)

The simplified fabrication process outlined in this paper is illustrated in figure 2. A 300 nm thick SiO_2 inter-level dielectric (ILD) is thermally grown at 1050 °C using a wet oxidation furnace. To protect the ILD layer during the chemical-mechanical-planarization (CMP) step, approximately 500 nm thick silicon-nitride (SiN) layer is deposited using plasma-enhanced-chemical-vapor (PECVD) as the CMP stop layer. Next, a 500 nm thick PECVD SiO_2 layer is deposited as the dielectric hardmask followed by deposition of a 100 nm thick Chromium (Cr) as the metal mask. The Cr mask is a transition hardmask used for etching 1.3–1.5 μm thick dielectric layers and for transferring the pattern from the soft-mask (EBL photoresist) to the dielectric hardmask. Next, a 900 nm thick ZEP520A photoresist is spin-coated on the Cr layer at 500 rpm for 60 s followed by a pre-exposure bake of 180 °C for 2 min using a hotplate (see figure 2(a)). The Cr mask enables etching of the 1.5 μm thick dielectric layers since EBL photoresist is not thick enough to etch the dielectric layers (based on its etch selectivity). Arrays of circular features are exposed with different doses to experimentally determine the proper base exposure dose. Figure 3(a) shows exposure dose versus the remaining thickness of photoresist in 75 × 75 μm square shape features after developing in Amyl Acetate for 2 min. These control features (i.e. dose squares) are designed to monitor photoresist thickness variations and required adjustments on the exposure dose. The optimum base dose is estimated to be 200 μC cm^{-2} considering the first fully developed dose square with sharp corners as shown in figure 3(b).

2.2. Hardmask etching

Fine resolution Cr mask dry etching (step (b) in figure 2) is performed using Chlorine (Cl_2), Oxygen (O_2), and Hydrogen (H_2) gases in an inductively coupled plasma (ICP) system [19]. Figure 4(a) shows Cr etch rate characterization for the dose squares using a profilmeter with respect to DC bias of the RF coil. Since the etch rate of the sub-micron features is slower than in the dose squares, 10% over etching is performed to ensure that the features are fully etched as shown in figure 4(b). Next, the remaining ZEP520A on the Cr mask is stripped off in 1165 solvent at 80 °C for 45 min prior to etching the SiO_2 mask. Eventually, the SiO_2 hardmask is dry etched using a mixture of fluorocarbon gases (C_4F_8 and CF_4), and O_2 in an ICP system [20].

2.3. Deep silicon etching

The Bosch process is dependent on the geometry of features being etched. Figure 5 shows an excessive undercut, poor selectivity, and pronounced sidewall roughness resulting from a standard Bosch etch of the sub-micron TSVs (step (c) in figure 2). To minimize undercut and increase mask-to-silicon etch selectivity, the process parameters should be adjusted accordingly. It is also important to achieve a relatively smooth sidewall with smaller scalloping as it could be crucial for high AR structures in different applications. For example, through modeling, it has been shown that excessive scalloping on the TSV sidewall impacts TSV reliability and electrical characteristic [21, 22].

The bosch process involves sequential etching and passivation cycles with different process parameters such as cycle duration, plasma power, chamber pressure, gases flow rate, and silicon substrate temperature. These process parameters non-linearly influence the overall etching performance, which makes the optimization procedure challenging to formulate. While there is significant effort in this space [23–26], some of the solutions for etching sub-micron size features exhibit limitations [27–30]. In this paper, an experimental approach is adopted for achieving reasonable etch results for the target application. To limit the possible number

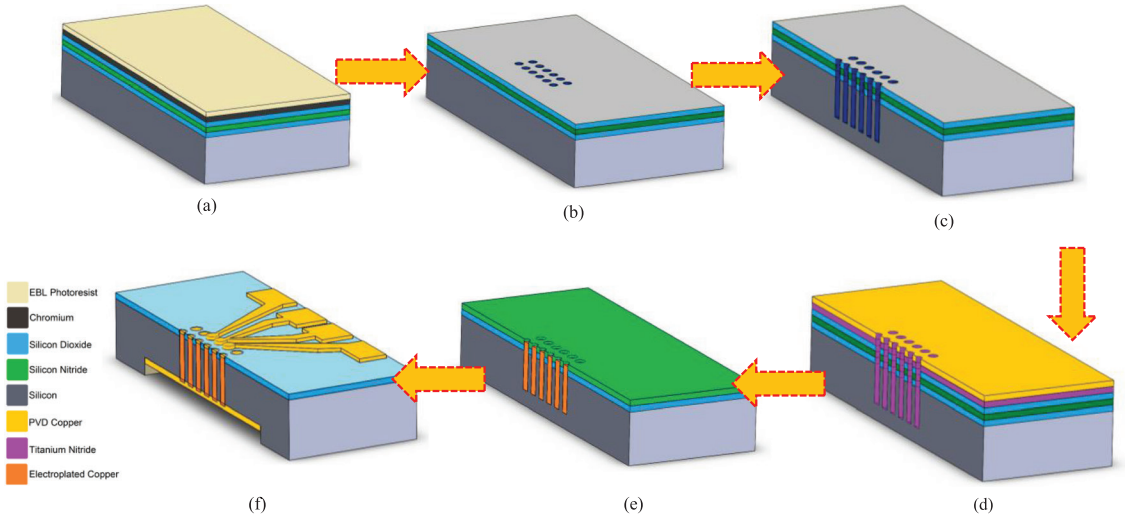

Figure 2. Fabrication process flow. (a) Deposition of: 1-SiO_2 ILD layer, 2-SiN CMP stop layer, 3-SiO_2 and Cr hardmasks 4-EBL photoresist layer followed by EBL lithography. (b) Cr mask etching and pattern transfer to SiO_2 hardmask. (c) Deep etching Si using the developed nano-Bosch process. (d) Deposition of: 1-SiO_2 liner 2-TiN diffusion barrier layer 3-Cu electrode layer. (e) Cu electrodeposition, followed by CMP. (f) TSV revealing followed by patterning and metallization of the pads and wires.

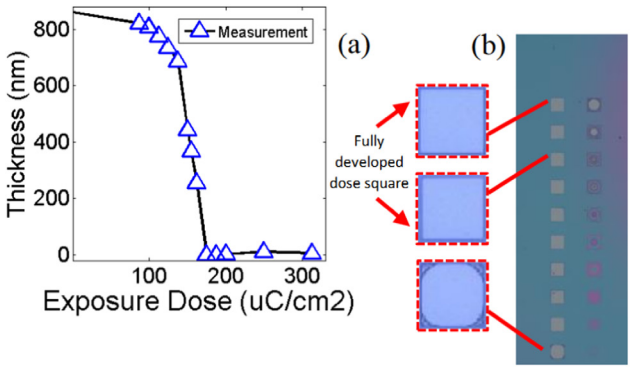

Figure 3. (a) Different exposure doses are applied to the sample to find the optimum dose. (b) Dose squares show photoresist remaining after development as a control procedure for monitoring required exposure dose.

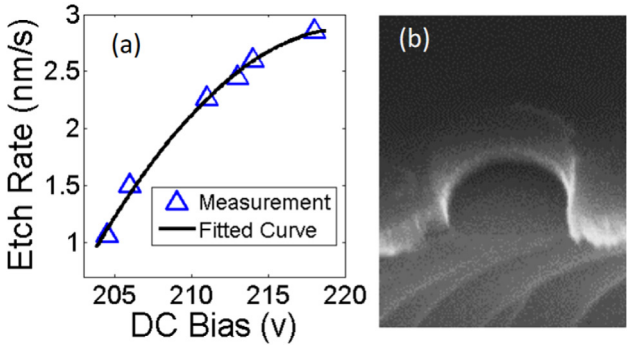

Figure 4. (a) Cr etching rate variation indicated by DC bias fluctuation. (b) SEM cross-section from dry etched features on the Cr hardmask.

of different combinations with the process parameters, only the effects of the passivation cycle duration, the etching cycle duration, and O_2 flow rate are explored in this effort. Adding O_2 to SF_6 in the etching cycle forms a thin SiO_xF_y passivation

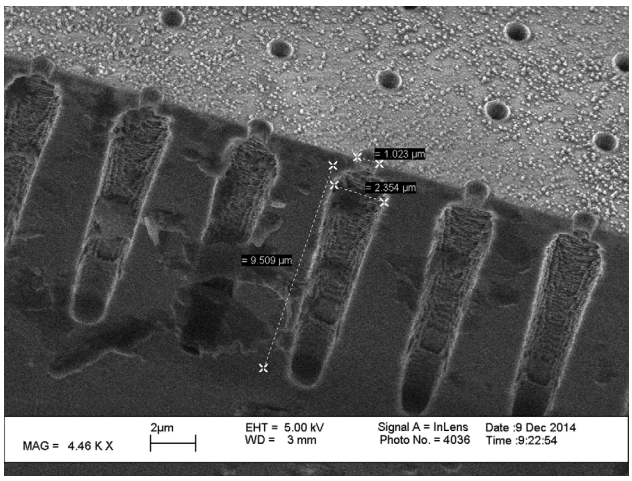

Figure 5. Standard Bosch etching introduces significant undercut and roughness to sub-micron diameter features.

film that improves anisotropic etching [31], which is believed to result in smaller undercut and a smoother sidewall [32]. Thus, two different flow rate ratios for SF_6 to O_2 are explored (as a function of etch-to-passivation cycle ratio) to observe undercut and selectivity behavior with all other process variables kept constant at the base conditions. Figure 6(a) shows that the smallest undercut is achieved at higher O_2 flow rates but the corresponding data point on the selectivity graph (figure 6(b)) does not demonstrate the highest achievable selectivity. However, minimizing undercut is a more critical objective since poor selectivity could be mitigated by depositing a thicker hardmask layer. Sidewall scalloping is simultaneously monitored for each experiment by cross-sectional SEM imaging. Figure 7 shows an etched silicon via that corresponds to the minimum undercut data-point in figures 6(a) and 31:1 selectivity. This reasonable selectivity and undercut results from longer passivation cycle with a higher O_2 content.

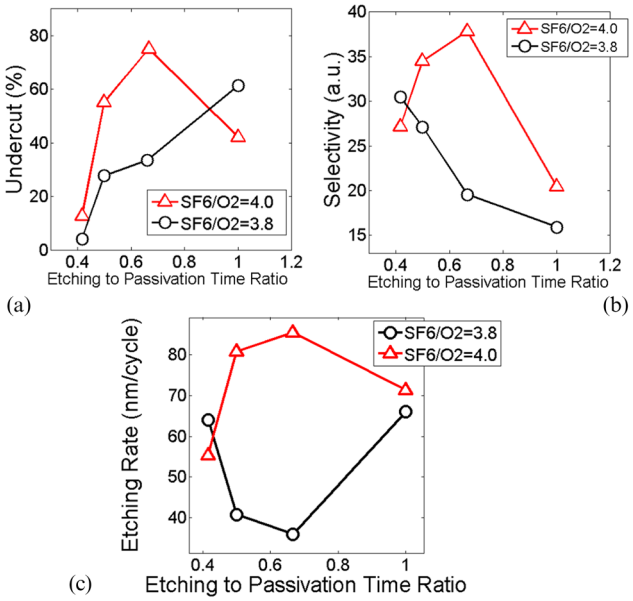

Figure 6. (a) Undercut versus etching/passivation ratio. (b) Selectivity versus etching/passivation ratio. (c) Silicon etching rate versus etching/passivation ratio.

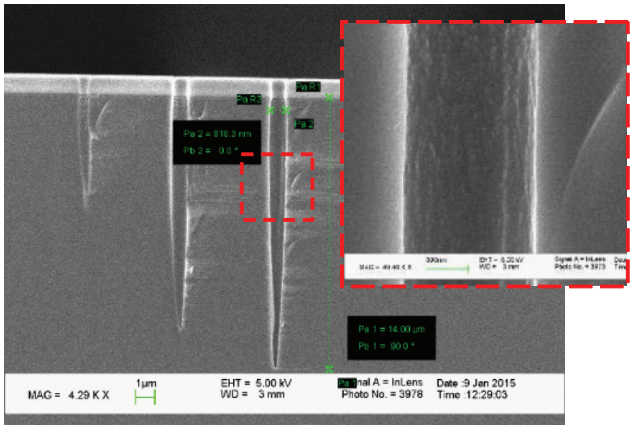

Figure 7. SEM cross-section of the sub-micron diamater via deep etched in silicon. No scalloping is observed in the magnified image.

2.4. Metallization

Void defects in the Cu core of the TSVs are a major manufacturing reliability concern, and thus, must be explored for the TSV under consideration. Depositing a diffusion-barrier layer along with a conductive seed-layer on the TSV sidewalls are the very first steps of the metallization process that significantly impact the subsequent Cu electrodeposition. Defect-free coverage of the seed-layer on the TSV sidewalls is important since any discontinuity of the film from the top to the bottom of the TSV could result in voids. Conventional PVD methods, such as sputtering, exhibit limitations for the conformal deposition of the diffusion-barrier film (e.g. TiN) and seed-layer (e.g. Cu) due to strong dependency of material deposition upon the via AR and diameter [10]. To address this issue, atomic layer deposition (ALD) is an attractive alternative for conformal film deposition in high AR trenches. Deposition of TiN—diffusion-barrier layer—using ALD for interconnects has been explored previously [33–35]. TiN is electrically

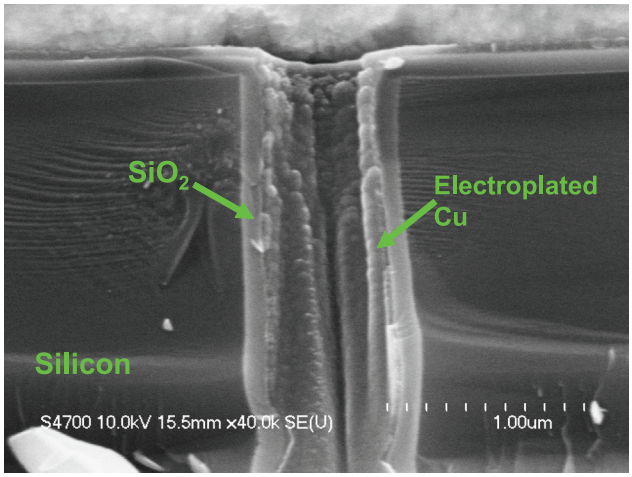

Figure 8. Cross-sectional image, shows that cupric ions are reduced on the TiN film and forming a layer of Cu on the TSV sidewall.

conductive, which opens the possibility for using it as both a diffusion barrier and a seed layer. However, the resistivity of TiN is large and thus forms a large series resistance over a large surface area which makes it challenging for use as a seed-layer on a large diameter wafer. Because the series resistance causes a non-uniform current density distribution over a large surface area, (e.g. 4-inch diameter silicon wafer) non-uniform electroplating results across the wafer. To address this limitation, a thin layer of Cu (approximately 100 nm) is evaporated on the TiN coated substrate (see figure 2(d)). It is important to emphasize that this Cu layer does not cover the TiN film on the TSV sidewalls but mostly only coats the top surface of the wafer. This not only bypasses the series resistance of TiN film, but also makes the subsequent Cu electrodeposition less dependent upon the thickness of the TiN layer. In this effort, ALD TiN is deposited on an SiO_2 liner using Cambridge NanoTech Plasma ALD tool (step (d) in figure 2). The employed precursors are (Tetrakis(dimethylamido) Titanium(IV)) (TDMAT) and NH_3 [34] processed at 250 °C. The thickness of the TiN film is measured to be approximately 45 nm using a Woollam M2000 Ellipsometer. To prove the concept, a test sample is partially electroplated for 10 min and cleaved for cross-sectional inspection. Figure 8 shows that cupric ions are reduced on the TiN film and form a layer of Cu on the TSV sidewall. This proves that the use of TiN is a feasible approach for metalizing scaled TSVs. Next, electrodeposition is performed on the sample (see figure 2(e)) using super-filling and reverse pulse plating (RPP) techniques [36–38]. The super-filling technique employs special additives in the electroplating electrolyte that accelerates Cu deposition in the bottom of the TSV while decreases Cu growth rate at the top. However, there are different electroplating bath chemistries and additives [39] that makes the experimental design space large. Thus, an electroplating bath (MICROFAB DVF 200) specialized for TSV processing [40] with two additive compounds, accelerator (Part 'B') and suppressor (Part 'C'), is employed as a starting point and the end result is shown in figure 9(a). It is believed that the bottom voids are formed due to large grain growth close to the TSV opening, causing pinching. This coarse Cu grain growth might be because of

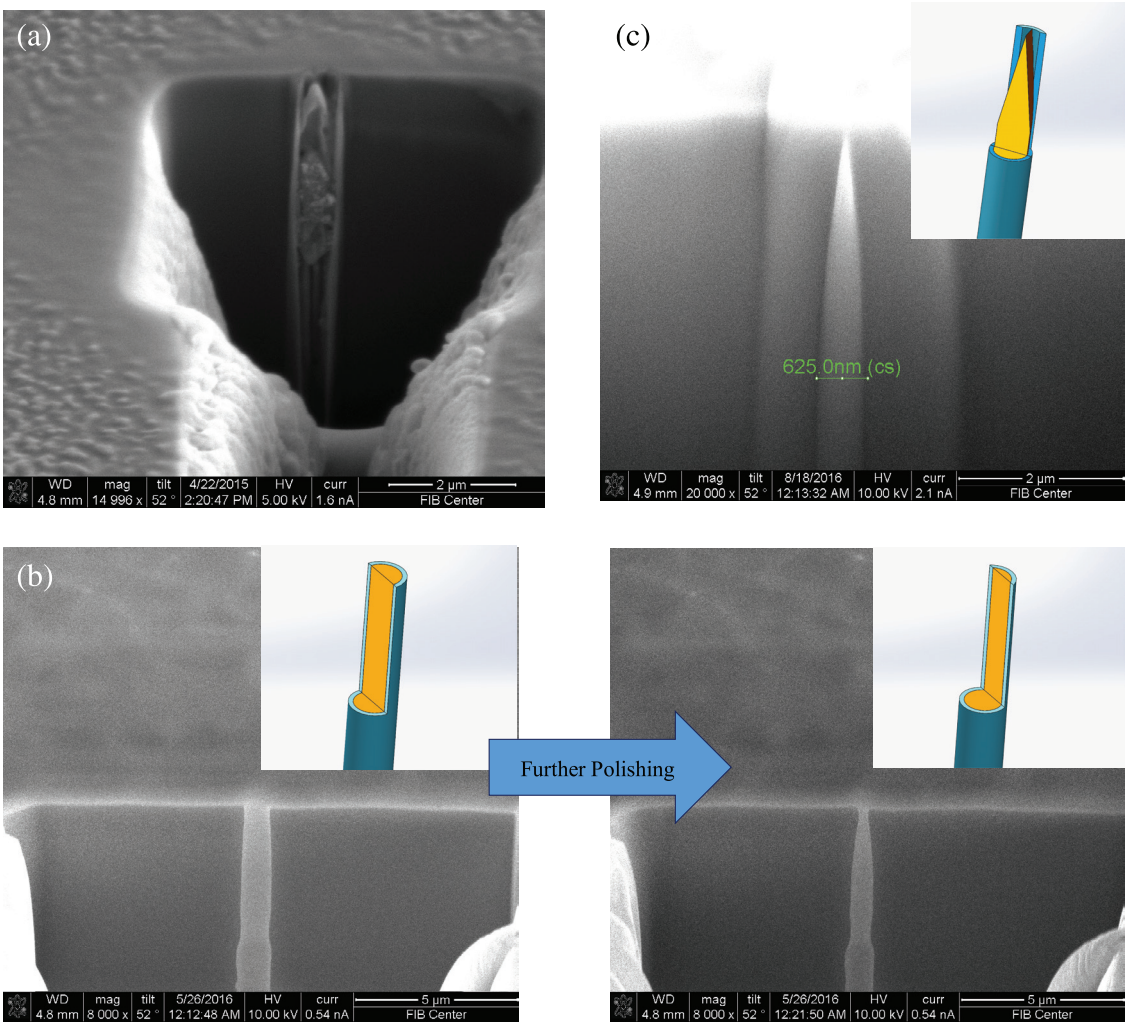

Figure 9. (a) SEM cross-section from the electropled TSV using MICROFAB DVF 200 plating bath that exhibits bottom-voids and a pinch-off at the TSV opening. (b) SEM cross-section at 50% and 30% depth from a sample electropled using TECHNIPULSE 5300 plating bath. (c) SEM cross-section from a sample resembling a needle due to FIB stage misalignment.

Table 1. Reverse pulse electroplating parameters.

Process parameter		Unit
Reverse cycle duration	2	ms
Reverse pulse duty cycle	50	%
Reverse pulse frequency	1000	Hz
Reverse current	Approx. 25	mA
Forward pulse duty cycle	50	%
Forward pulse frequency	200	Hz
Forward cycle duration	25	Mims
Forward current	Approx. 15	mA
Agitation	200	RPM
Bath temperature	Approx. 23	°C

the bath chemistry and additives concentration that are optimized for fast electroplating of TSVs with diameter ranging from 5 μm to 20 μm [41, 42]. To test this hypothesis, another electroplating bath (TECHNIPULSE 5300) that is designed for finer grain deposition of Cu [43] has been explored using the electroplating parameters shown in table 1. The cross-sectional TSV FIB image shown in figure 9(b) resulting from this bath chemistry exhibits no Cu voids and is a significant improvement. To ensure the imaged sample is defect free, polishing is continued to the deeper regions as shown in figure 9(b). It is important to note there were a number of challenges associated with the cross-sectioning of high AR TSVs; for instance, the sample should be perfectly perpendicular to the ion-beam and any small stage misalignment causes non-uniform FIB milling. In figure 9(c), it is shown that the cross-section of the Cu core resembles a needle due to a higher removal rate at the top. Moreover, simultaneous milling of 3 different materials (silicon, SiO_2, and Cu) is complex as they have different hardness. Although no voids are observed in the cross-sectioned samples regardless of these imaging challenges, we are aware that significantly larger visual data set is needed to demonstrate the manufacturing yield.

3. Electrical characterization

3.1. Electrical resistance

To characterize electrical resistance (R_{TSV}) of the fabricated TSVs in section 2, the back side of the silicon substrate is aligned with the topside features (e.g. TSVs) and patterned using optical lithography. Next, the patterned features (i.e.

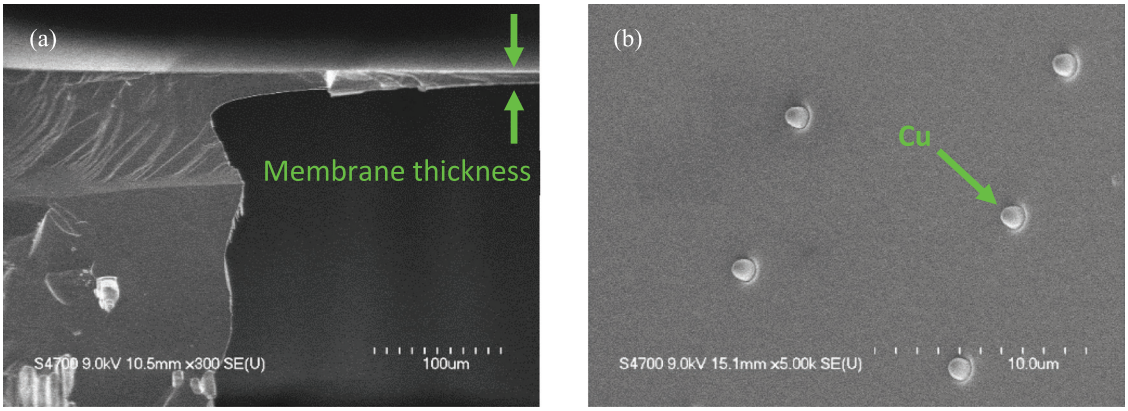

Figure 10. (a) SEM cross-section from the backside etched silicon substrate that shows 285 μm deep cavity. (b) SEM image from the revealed end of TSVs after backside etching shows the Cu core of TSVs.

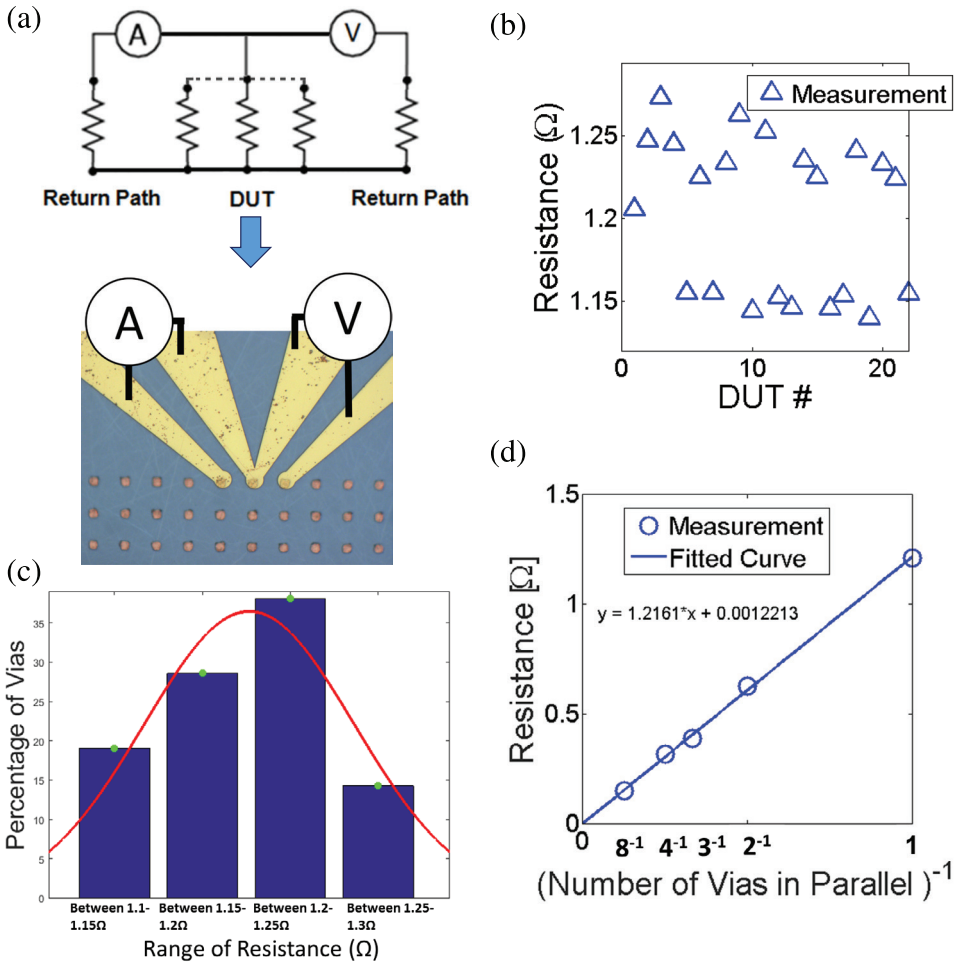

Figure 11. (a) Schematic of the 4-wire Kelvin probe technique for characterizing the DUT in the test-vehicle. (b) Measured R_{TSV} of DUTs approximately ranging from 1.14 Ω to 1.27 Ω. (c) Gaussian distribution of the measured R_{TSV} for different DUTs. (d) R_{TSV} measured for 2, 3, 4, and 8 parallel TSVs.

openings) on the back side are dry etched (see figure 2(f)) to reveal the blind end of the TSVs. This creates a cavity with approximately 285 μm depth (for a 300 μm thick silicon wafer), as shown in figure 10(a). Figure 10(b) shows the TSV Cu core revealed after backside etching. Next, the closed electrical loop is formed by shorting the revealed end of the TSVs by sputtering a layer of Cu into the cavity. The probing pads and wires for electrical characterization are patterned using EBL and the metal layers—Ti/Cu/Au (30 nm Ti, 1 μm Cu, and 350 nm Au)—are deposited using a sputtering tool for good step coverage.

Next, R_{TSV} of 15 μm deep TSVs with approximately 680 nm diameter Cu core is measured using the four-wire Kelvin probe technique as shown in figures 11(a) and (b). Figure 11(c) illustrates a Gaussian distribution of the measured R_{TSV} for different DUTs. The average measured R_{TSV}

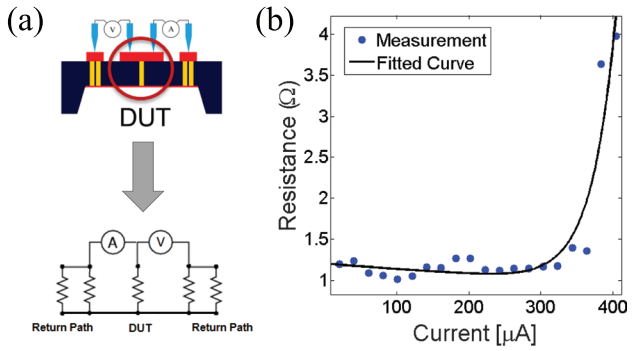

Figure 12. (a) Schematic of the test-vehicle designed for measuring CCC. (b) Current carrying capacity is measured for sub-micron TSVs by pumping current through the DUT and monitoring its resistance.

is calculated to be approximately 1.2 Ω. Furthermore, R_{TSV} for 2, 3, 4, and 8 parallel TSVs is measured and plotted in figure 11(d). The slope of the fitted curve suggests that the extracted average R_{TSV} for a single TSV is 1.216 Ω which agrees with the measured R_{TSV}. Given the fabricated TSV dimensions, Cu resistivity of the metal core is extracted to be approximately 2.95 μΩ cm. It is shown by Chang *et al* [44] that the use of the chosen additives in the electroplating bath chemistry increases Cu resistivity from 2 μΩ cm to 2.9 μΩ cm. This agrees with the measurements presented in this paper.

3.2. Current-carrying capacity

Figure 12(a) illustrates the schematic of the test vehicle that is designed to measure the current-carrying capacity (CCC) of the sub-micron TSVs fabricated in section 2. The CCC measurement is conducted by monitoring R_{TSV} while DC current is pumped into a single TSV (i.e. DUT). To decrease the return path electrical resistance, eight TSVs are connected in parallel for this experiment. This ensures that the current flow is not limited in the return path. Next, the DC current is increased until R_{TSV} exhibits a rapid change ($\Delta R_{TSV}/R_{TSV} \geqslant 20\%$), indicating that the DUT has reached its maximum CCC (i.e. ampacity). The measurements shown in figure 12(b) suggest that the ampacity of the DUT is 360 μA, or 105 kA cm^{-2}.

4. Conclusion

In this paper, we reported enabling fabrication processes for sub-micron TSVs to gain the most from the connectivity benefits (e.g. low parasitic capacitance) of fine-grain 3DI. The presented sub-micron TSV technology enables heterogeneous 3D ICs using vertically stacked thin silicon tiers. The demonstrated approximately 900 nm diameter TSVs are 15 μm deep with 680 nm Cu core. To address the challenges in fabricating these TSVs, nano-Bosch silicon etching with no scalloping and direct Cu super-filling on a TiN diffusion barrier layer have been developed as the two key enabling modules. Furthermore, using the test-vehicle, the average electrical resistance of these sub-micron vias is measured to be approximately 1.2 Ω. Furthermore, maximum CCC of the scaled TSVs is characterized to be approximately 360 μA. Given TSV dimensions, the current density at maximum CCC and Cu resistivity are extracted to be approximately 105 kA cm^{-2} and 2.95 μΩ cm, respectively.

Acknowledgments

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